FUNCTIONAL CONTROL TECHNIQUE FOR FPGA TOTAL IONIZING DOSE TESTING

D.V. Bobrovsky, O.A. Kalashnikov, P.V.Nekrasov.

Abstract – The TID FPGA functional control methodology is described. The necessity of 100% FPGA functional blocks testing is demonstrated. Experimental results for FPGA AX1000, EPF10K50, and A3PE600L are shown.

I. Introduction

There are three common techniques of forming a programmable connection in FPGA: RAM, Flash and Antifuse. FPGA can be divided in two parts: the service area - a block of memory, which stores configuration information and the user area, consisting of logical resources available to the user.

The information written in the configuration memory determines the function performed by the scheme; therefore, a change of this information leads to functional failures. A possibility to overwrite the configuration information is also an important parameter.

TID effects in FPGAs appear as parametric failures associated with increasing current, degradation of the output and input logic levels, changing the dynamic characteristics of the circuit. And as a functional failure of any block, for example:

1. Failure of configuration memory as a result leads to complete loss of FPGA's working capacity. This is due to the loss of information in cells or to the effect of data "sticking", which leads to the FPGA reconfiguring inability;
2. Failures in blocks of user memory (RAM, Flash). It leads to the loss of information or inability to overwrite it.
3. Failures in the storage elements of logic cells.
4. Failures in combinational circuits (multiplexers, arithmetic logic, etc.).
5. Failures in the peripheral functional blocks, such as PLL, DSP, Ethernet-controller, etc.

It is not known in advance which functional unit will fail. There for it is not allowed to conduct the functional control of the scheme using a multi-digit counter, even with 100% resources utilization. This can lead to significant overestimation of the TID hardness level. To solve this problem, we propose a method independent of functional control of the FPGA's basic elements.

The work was supported by Russian Science and Education Ministry within "Complex-MEPHI" project under Russian Federation Government Regulation №218.

Oleg A. Kalashnikov is with National Research Nuclear University (NRNU) "MEPHI",Moscow, Russian Federation (e-mail: oakal@spels.ru).

Dmitry V. Bobrovsky is with Specialized Electronic Systems (SPELS),Moscow, Russian Federation (e-mail: dvbob@spels.ru)

Pavel V. Nekrasov is with National Research Nuclear University (NRNU) "MEPHI",Moscow, Russian Federation (e-mail: pvnek@spels.ru).

II. Testing method

The method is based on the selection of elementary functional blocks (primitives) in the FPGA. For each type of functional unit a test unit is created so all the basic blocks of the FPGA are tested without correlation.

With the regularity in FPGA structure the same basic functional blocks within the same class or family of FPGAs and a large number of similar elements could create a library of test blocks. Creating such library in VHDL allows easy switching between different FPGA vendors or families.

Implementation of the method begins with the FPGA architecture analysis and the basic function blocks allocation.

The basic blocks should be selected as follows: LUT, storage element, multiplexer, arithmetic logic, block memory, configuration memory, input/output blocks.

As a basic block is selected available resources should be estimated (memory, number of storage elements, etc.) in order to determine the library element parameters such as size of the memory block, the length of the test chain of flip-flops, etc. Selected units are grouped into a single test firmware. Thus, there is a functional control of all basic elements of the FPGA.

During test procedure the software components are activated in accordance with a set of blocks included in the FPGA firmware.

III. Testing Devices

To evaluate the efficiency of the proposed method were conducted comparative research of two FPGA types firmware, universal and specialized counter type.

The devices under test were EPF10K50 (Altera), AX250 (Actel) and A3PE600L (Actel).

The scheme of multi-digit counter was used as a universal test firmware. Basic blocks have been selected and the corresponding test firmware has been formed for the method of independent functional control.

All circuits were tested using 1,5 MeV electron accelerator U-31/33 and 40 KeV X-ray source REIM-2 (SPELS, Russia). A full parametric control, including output logic levels, static and dynamic current, the switching characteristics and dynamic parameters of the trigger logic cells was carried out during the research.

IV. Radiation Test Results.

FPGA EPF10K50. The first functional failure at 30 krad (Si) was characterized by the "sticking" of all memory cells (Figure 1). The logic storage elements failed later (36 krad). This failure is associated with degradation of the trigger dynamic parameters which leads to an 10% shift time increase.

No other failures were observed including the functional control with the simplified method.

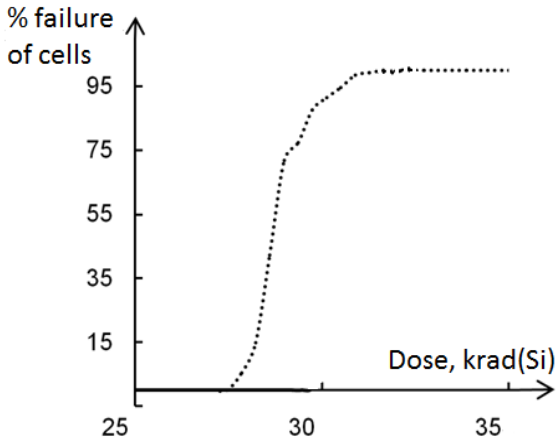

Fig. 1 FPGA EPF10K50 memory cells failure vs total dose

FPGA AX250. Only PLL failure was observed with TID level exceeding 190 krad. PLL output frequency vs total dose is shown in Fig. 2.

FPGA A3PE600L. First functional failure at 50 krad was characterized by the violation of the custom flash-memory, operating in read mode. Second failure (54 krad) of the configuration memory resulted in failure of block RAM, counter, and the multiplier. PLL failed at 85 krad.

V. Data analysis

Table 1 shows the experimental results of three FPGA EPF10K50, AX250, and A3PE600L irradiation. The tested function blocks, the time of functional failure and the failed unit are shown in Table 1.

In all three cases, the simplified test firmware does not lead to correct functional failure TID level.

These examples confirm the importance of functional control with the simplified test firmware inadmissibility and high reliability of the independent FPGA functional control method. It allows identifying functional failure along with the failed unit.

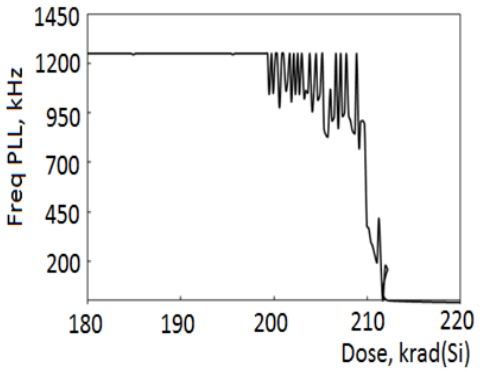

Fig. 2 PLL output frequency vs total dose

Table 1. FPGA EPF10K50, AX250, and A3PE600L TID failure test results

EPF10K50					
Dose, ×103 krad(Si)	Counter	Shift register	Flip-flop	Multiplexor	Block memory
24	+	+	+	+	+
28	+	+	+	+	—
32	+	+	+	+	—
36	+	+	—	+	—
40	+	+	—	+	—
AX250					
Dose, ×103 krad(Si)	Counter	Block memory	PLL	Flip-flop	Multiplier
200	+	+	+	+	+
220	+	+	—	+	+
350	+	+	—	+	+
A3PE600L					
Dose, ×103 krad(Si)	Counter	Block memory	Flash ROM	Flip-flop	PLL	Multiplier
48	+	+	+	+	+	+
50	+	+	—	+	+	+
54	+	—	—	+	+	+
56	+	—	—	+	+	+
60	—	—	—	—	+	—
85	—	—	—	—	—	—

VI. References

1. Clark, S.L. TID and SEE testing results of Altera Cyclone field programmable gate array/ S.L. Clark, K. Avery, R. Parker// 2004 IEEE Radiation Effects Data Workshop, 2004.- P.88- 90.

2. Wang, J.J. Radiation effects in FPGA's/J.J.Wang//Actel Corporation.- 2004.